REMARKS

This paper is filed in response to the Office Action mailed on May 2, 2005 therefore no extension of time fee is due. Claims 1, 5 and 9 have been amended; claims 2-4, 6-8 and 10-14 have been canceled; claims 1, 5 and 9 remain pending.

Turning to the rejections based on the prior art, claims 1 and 2 stand rejected under 35 U.S.C. 102(e) as being unpatentable over U.S. Patent No. 6,650,168 ("Wang"). In response, claim 1 has been amended and claim 2 has been cancelled. Applicants respectfully submit that claim 1 is not anticipated by Wang for the following reasons.

> At the outset, Under MPEP § 2131,
>
> "[t]o anticipate a claim, the reference must teach every element of the claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference."

Citing, Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Amended claim 1 recites a PMOS transistor driven according to the data signal directly inputted to the PMOS transistor from a peripheral circuit and connected to a power supply voltage terminal; a low voltage-driven NMOS transistor driven according to the data signal directly inputted to the low voltage-driven NMOS transistor from the peripheral circuit and connected to the PMOS transistor, wherein the low voltage-driven NMOS transistor having a threshold voltage of 0V; a NMOS transistor connected between the low voltage-driven NMOS transistor and a ground voltage terminal, wherein the NMOS transistor is turned on according to an output enable signal; and a latch unit for inverting and restoring a signal received via the PMOS transistor or the low voltage-driven NMOS transistor.

However, Wang does not teach or even suggest the low voltage-driven NMOS transistor driven according to data signal directly inputted from the column multiplexer. Wang merely discloses a first and second zero threshold voltage NMOS transistors. The zero threshold NMOS transistors of Wang are not driven by directly inputted signal from the peripheral circuit. Instead, the zero threshold NMOS transistors of Wang are driven by an inverting signal.

As a result, because the NMOS transistor of amended claim 1 is driven by a directly inputted signal, the NMOS transistor of amended claim 1 is different from the zero threshold NMOS transistors of Wang which are driven by the inverting signal and therefore Wang cannot serve as an anticipating reference for amended claim 1.

Wang also fails to teach or even suggest a NMOS transistor connected between the low voltage-driven NMOS transistor and the ground voltage terminal as recited in amended claim 1. Wang further fails to teach or even suggest a latch unit for inverting and restoring a signal received via the PMOS transistor or the low voltage-driven NMOS transistor as recited in amended claim 1. Finally, claim 1 relates to an input/output buffer and Wang merely relates to a level shifter. Thus, Wang cannot anticipate claim 1 for these additional reasons.

Next, claims 1 and 5 are rejected under 35 U.S.C. 102(e) as being unpatentable over U.S. Patent No. 6,542,011 ("Onishi"). In response, claims 1 and 5 have been amended to traverse this rejection.

Amended claim 1 recites a low voltage-driven NMOS transistor. In contrst, Onishi recites a plurality of FETs having a low threshold voltage, but no NMOS transistors driven by a low voltage. According to Onishi, a PFET (41), NFETs (42 and 43) are transistors all having a low threshold voltage. The Onishi FETs do not anticipate the low voltage-driven NMOS transistor limitation of amended claims 1 and 5.

Also, Onishi does not teach or even suggest the latch unit for inverting and restoring a signal received via the PMOS transistor of amended claim 1 or the low voltage-driven NMOS transistor of amended claims 1 and 5. The Patent Office takes the position that the PFET (44) and the inverter (45) of Onishi are a latch unit. However, Onishi's inverter (45) and PFET (44) perform a latch operation only when the input signal of the inverter (45) is at a high level. In contrast, amended claim 1 recites a latch operation regardless of the input signal, i.e. either the PMOS transistor or the low voltage-driven NMOS transistor and therefore Onishi cannot anticipate amended claim 1.

Amended claim 5 recites a first logical element driven according to a data signal directly inputted to the first logical element from a peripheral circuit, the first logical element having a PMOS transistor and a low voltage-driven NMOS transistor; a second logical element for inverting and restoring a signal received via the PMOS

transistor or the low voltage-driven NMOS transistor; and a NMOS transistor that is connected between the low voltage-driven NMOS transistor and a ground voltage terminal with the switching element being turned on according to an output enable signal, wherein the low voltage-driven NMOS transistor having a threshold voltage of 0V. Onishi fails to teach these elements.

Therefore, Onishi fails to teach or suggest every element of amended claims 1 or 5 and therefore the anticipation rejection of these claims is improper and should be withdrawn.

Next, Claims 2-4 and 6-8 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Onishi. However, claims 2-4 and 6-8 have been cancelled rendering this rejection moot. Further, Under MPEP § 2142,

> "[t]o establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally availableto one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimedcombination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. "

Citing, In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); *see also* MPEP § 2143-§ 2143.03 for decisions pertinent to each of these criteria. As established above, Onishi fails to each or suggest every claim element of amended independent claims 1 and 5 and therefore no *prima facie* of obviousness of claims 1 or 5 in view of Onishi has been established.

Finally, claims 9-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,842,377 (Takano") in view of Onishi. Claims 10-14 have been cancelled and therefore only amended claim 9 is at issue.

Amended claim 9 recites a data input/output buffer for storing the data selected by the column multiplexer and transferring the data to a data line, wherein the data input/output buffer comprises a PMOS transistor driven according to the data signal directly inputted to the PMOS transistor from the column multiplexer and connected to a

power supply voltage terminal; a low voltage-driven NMOS transistor driven according to the data signal directly inputted to the low voltage-driven NMOS transistor from the column multiplexer and connected to the PMOS transistor, wherein the low voltage-driven NMOS transistor having a threshold voltage of 0V; a NMOS transistor connected between the low voltage-driven NMOS transistor and a ground voltage terminal, wherein the NMOS transistor is turned on according to an output enable signal; and a latch unit for inverting and restoring a signal received via the PMOS transistor or the low voltage-driven NMOS transistor.

The deficiencies of Onishi are discussed above. Takano only discloses a memory cell array, a row decoder and a page buffer and cannot be used to cure the deficiencies of Onishi. Clearly neither Takano nor Onishi teach or even suggest the second logic element for inverting and restoring a signal received via the PMOS transistor or the low voltage-driven NMOS transistor. Therefore, amended claim 9 is clearly patentable over any hypothetical combination of Takano and Onishi.

The Commissioner is authorized to charge any fee deficiency required by this paper, or credit any overpayment, to Deposit Account No. 13-2855.

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